CLAIMS

1. A precision margining circuit, comprising:

a first margining resistor coupled between first and second margining nodes;

a first offset resistor coupled between said second margining node and a supply reference node;

a first amplifier circuit that drives current to said first margining node to establish a reference voltage at said second margining node;

a second amplifier circuit that mirrors a first margining voltage developed between said first and second margining nodes across a second margining resistor to develop a first margining current; and

a feedback circuit that adjusts a set point voltage based on said reference voltage and said first margining current.

2. The precision margining circuit of claim 1, wherein said first amplifier circuit comprises:

an amplifier having a first input receiving said reference voltage, a second input coupled to said second margining node and an output; and

a current device having a current control input coupled to said output of said amplifier and a current path coupled to said second margining node.

3. The precision margining circuit of claim 1, further comprising:

a current mirror having a current path input that senses said first margining current and a current path output that drives proportional current through a third margining resistor to develop a second margining voltage; and

a summing circuit that adds said reference voltage to said second margining voltage to adjust said set point voltage.

4. The precision margining circuit of claim 1, further comprising:

a second offset resistor coupled between said first margining node and said supply reference node;

select logic, responsive to a margining control node having up and down states to switch between applying up and down margining, that couples an output and a feedback input of said first amplifier circuit to said first and second margining nodes, respectively, in said up state and that couples said output and said feedback input of said first amplifier circuit to said second and first margining nodes, respectively, in said down state;

said second amplifier circuit being enabled when said margining control node is in said up state;

a third amplifier circuit, enabled when said margining control node is in said down state, that mirrors a second margining voltage developed between said first and second margin nodes across a third margining resistor to develop a second margining current; and

said feedback circuit adjusting said set point voltage based on said reference voltage and said first and second margining currents.

5. The precision margining circuit of claim 4, wherein said first, second and third amplifier circuits, said select logic and said feedback circuit are implemented on a common integrated circuit (IC), wherein said first and second margining nodes and said margining control node are implemented as pins on the IC.

6. The precision margining circuit of claim 4, further comprising a margining capacitor coupled between said first and second margining nodes.

7. The precision margining circuit of claim 4, further comprising:

first and second current mirrors having current path inputs that sense said first and second margining currents, respectively, and current path outputs that drive proportional currents through fourth and fifth margining resistors to develop second and third margining voltages, respectively; and

said feedback circuit incorporating said fourth and fifth margining resistors and adjusting said set point voltage based on said second and third margining voltages.

8. The precision margining circuit of claim 4, wherein said second and third amplifier circuits each comprise:

a first buffer amplifier that drives a current device to drive current through a first end of a corresponding one of said second and third margining resistors based on voltage developed at said output of said first amplifier circuit; and

a second buffer amplifier that drives a second end of said corresponding margining resistor based on voltage developed at said feedback input of said first amplifier circuit.

9. An integrated circuit (IC), comprising:

a margining control amplifier circuit that drives current at an output to control voltage at an input based on a reference voltage;

first and second offset pins for coupling to an external margining voltage divider;

a margining control pin having at least two states including an up state and a down state;

select logic that selectively switches said output of said margining control amplifier circuit between said first and second offset pins and that selectively switches said input of said margining control amplifier circuit between said second and first offset pins based on a state of said margining control pin; and

a mirror amplifier circuit that mirrors voltage across said first and second offset pins across a first margining resistor.

10. The IC of claim 9, wherein said select logic comprises:

a first switch having a common pole coupled to said input of said margining control amplifier circuit, first and second switched terminals coupled to said first and second offset pins, respectively, and a control input coupled to said margining control pin; and

a second switch having a common pole coupled to said output of said margining control amplifier circuit, first and second switched terminals coupled to said first and second offset pins, respectively, and a control input coupled to said margining control pin.

11. The IC of claim 9, further comprising:

a first up margining resistor and a first down margining resistor;

an up amplifier circuit, enabled by said margining control pin when in said up state, that mirrors voltage between said first and second offset pins across said first up margining resistor; and

a down amplifier circuit, enabled by said margining control pin when in said down state, that mirrors voltage between said first and second offset pins across said first down margining resistor.

12. The IC of claim 11, wherein said up and down amplifier circuits each comprise:

a first amplifier having an inverting input coupled via said select logic to said controlled current path of said current device, a non-inverting input coupled to a first end of a corresponding one of said first up and down margining resistors, and an output;

a second current device having a current control input coupled to said output of said first amplifier and a controlled current path coupled between a source voltage and said non-inverting input of said first amplifier; and

a second amplifier having an inverting input and an output coupled to a second end of said corresponding one of said first up and down margining resistors and a non-inverting input coupled via said select logic to said input of said margining control amplifier circuit.

13. The IC of claim 12, further comprising:

an up current mirror having a current path input coupled in series with said first up margining resistor and a current path output;

a down current mirror having a current path coupled in series with said first down margining resistor and a current path output;

a second up margining resistor coupled to said current path output of said up current mirror for developing an up margining voltage; and

a second down margining resistor coupled to said current path output of said down current mirror for developing a down margining voltage.

14. The IC of claim 13, further comprising a feedback circuit that adjusts a set point voltage based on said reference voltage and said up and down margining voltages.

15. The IC of claim 14, wherein said feedback circuit further comprises:

a summing circuit that combines said reference voltage and said up and down margining voltages;

an operational transconductance amplifier (OTA) having an input coupled to said summing circuit and an output providing said set point voltage; and

an error amplifier that controls a compensation signal based on a sampled output voltage and said set point voltage.

16. The IC of claim 15, further comprising a soft start pin coupled to said output of said OTA for coupling an external soft start capacitor.

17. A method of precision margining control for a regulator, comprising:

coupling a margining resistor between first and second nodes and coupling a first offset resistor between the second node and a power supply terminal;

applying a current to the first node to maintain voltage at the second node at a reference voltage level;

mirroring voltage developed across the margining resistor across a second margining resistor; and

adjusting a set point voltage of the regulator based on the reference voltage and the margining current developed through the second margining resistor.

18. The method of claim 17, wherein said adjusting a set point voltage comprises:

mirroring current through the second margining resistor into an offset resistor that develops an offset voltage relative to the reference voltage; and

adding the offset voltage to said reference voltage.

19. The method of claim 17, further comprising:

coupling a second offset resistor between the first node and the power supply terminal;

selecting between the first and second nodes for selecting between up and down margining; and

said applying a current comprising applying current to a selected one of the first and second nodes to maintain voltage at a non-selected one of the first and second nodes at a reference voltage level.

20. The method of claim 19, wherein said mirroring voltage comprises mirroring voltage developed across the margining resistor across an up margining resistor when up margining is selected and across a down margining resistor when down margining is selected.

21. The method of claim 20, further comprising:

mirroring current through the up margining resistor into a first offset resistor that develops a positive offset voltage relative to the reference voltage; and

mirroring current through the down margining resistor into a second offset resistor that develops a negative offset voltage relative to the reference voltage.

22. The method of claim 21, wherein said adjusting a set point voltage comprises adding a selected one of the positive and negative offset voltages to the reference voltage.